ABSTRACT OF THE DISCLOSURE

Each memory block of a memory device a plurality of memory cells connected to a plurality of bit line pairs, a column selecting circuit, and a pre-charge and write control circuit. The column selecting circuit includes a plurality of CMOS transmission gates, each CMOS transmission gate including an NMOS transistor connected between one bit line of a bit line pair and a sense bit line of a sense bit line pair, and a PMOS transistor connected between the one bit line and one of the write bit lines of a write bit line pair. During a write operation, only the NMOS transistor of a selected one of the CMOS transmission gates is turned on, and the PMOS transistor of the selected CMOS transmission gate and the PMOS and NMOS transistors of all of the CMOS transmission gates except the selected one are all turned off.